

VIA Nano™ X2 E-series Processor

Overview



The VIA Nano™ X2 E-series processor is a dual core, super scalar, out-of-order architecture and is manufactured using advanced 40nm CMOS technology. This architecture and process technology provides a highly compatible, high-performance, and low-power consumption solution for any computing market.



High-Performance Computation and Media Processing

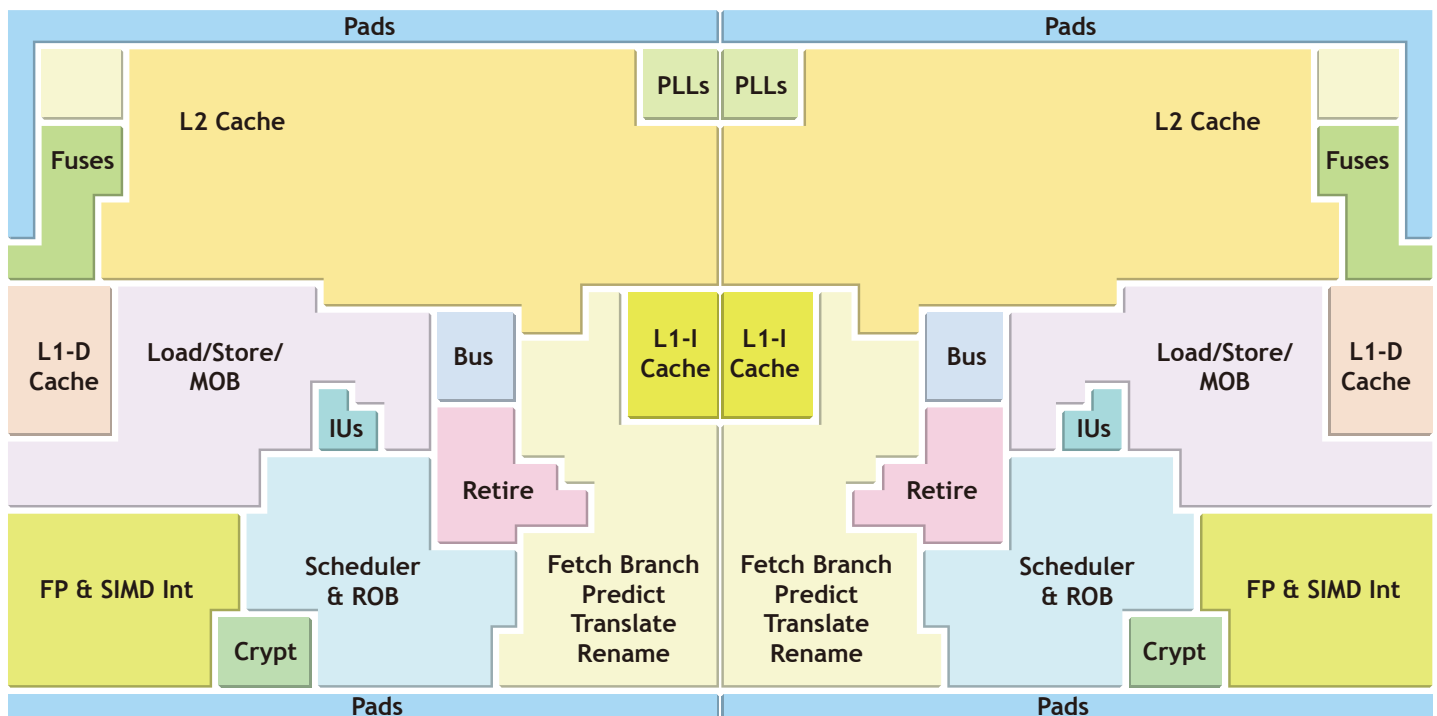
A high-speed, low power VIA V4 Front Side Bus at 800 / 1066MHz coupled with a high floating point unit, support for new SSE instructions, and two 64KB L1 caches and 2MB exclusive L2 cache with 16-way associativity offers huge gains in multimedia performance, including the latest multimedia and HD video codecs.

High-Performance Floating-Point Execution

The VIA Nano™ X2 E-series processor has been designed with significant emphasis on high-performance floatingpoint execution, using a completely new algorithm for floating-point adds that results in the lowest floating-point add latency of any x86 processor. Similarly, the floating-point multiplier has the lowest latency of any x86 processors.

PadLock

- Advanced Cryptography Engine: ACE
Padlock's Advanced Cryptography Engine provides the world's fastest AES encryption implementation. Wherever AES software encryption implementations are used today, it can be optimized for ACE with minimal effort. World class AES performance is a user-level instruction away as only one opcode handles encrypt and decrypt functions.
- Random Number Generator: RNG
VIA Nano™ X2 processor incorporate two random number generators on the processors die for a fast source of entropy.
- Secure Hash Algorithm: SHA-1 and SHA-256



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Key Features

Superscalar, Out-of-order X86 Architecture

- X86 and x64 (64bit) capability
- Software-compatible with thousands of x86 software applications available

CPU SKU

- L4350E 1.6+GHz @ 27.5W
- V4300E 1.2+GHz @ 13W

Front Side Bus (FSB)

- Bus speeds 1066MHz

Virtualization Technologies

- Hardware Virtualization (VMX)
- VIA Virtualization (VIA-VT)

Power Management

- Enhanced PowerSaver provides fastest performance state switching
- Low power consumption

Crypto

- World's fastest AES encryption using the Advanced Cryptography Engine (ACE)
- Secure Hash Algorithm: SHA-1 and SHA-256
- Random Number Generator
- Montgomery's Algorithm

Thermal Monitor

- Thermal Monitor 1, Thermal Monitor 2, and Catastrophic Thermal Protection

Multi Processor

- Multi-processor support: Dual processing (SMP)

Instruction Sets

- MMX, SSE, SSE2, SSE3, SSSE3, and SSE4.1-compatible instructions

On-die Cache

- Two large (64-KB each, 16-way) Level 1 caches per core
- 1 MB Level 2 victim cache (32-way) with ECC per Core (2MB total)
- Advanced L2 Hardware Prefetch
- Two large TLBs (196 entries each, 12-way)
- Branch Target Address Cache with 4096k entries
- Unique and sophisticated branch prediction mechanisms

Package

- Flip-Chip Ball Grid Array (FCBGA)
- Pin compatible with previous generation
- Package Size: 21x21mm

